LBS COLLEGE OF ENGINEERING, KASARAGOD

Tender Notice

Tender No. D-1156/2021- BSK 34 **Date: 07.10.2022**

Sealed competitive tenders are invited by the Principal, LBS College of Engineering, Kasaragod from the authorized dealers for the supply of **DSP Trainer Kit** for ECE Department in LBS College of Engineering, Kasaragod.

Description of item:-

The supply of the item should be as per the details given in the schedule

1. Period of completion of supply and installation within 30 Days from the date of supply order.
2. Cost of Tender form : Rs.500
3. EMD : Rs. 1500./-
4. Last date of sale of Tender form : 07.11.2022, 4 P.M
5. Last date of submission of Tender : 08.11.2022, 2 P.M
6. Date of opening Tender : 08.11.2022, 3 P.M
7. Validity of the Tender : 6 Months

Sale of Tender document : The complete set of Tender documents can be received from The Principal, LBS College of Engineering, Kasaragod on submission of a written application along with a non refundable fee of Rs. 500/- (Rupees Five Hundred only) in cash or DD.

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1. College Website
2. Notice Board

Specifications of DSP Trainer kit (3 nos)

TMS320C6748 BASED DSP TRAINER KIT [MODEL: VSK – 6748]

The C6748 is a low-power digital signal processor based on C674x DSP core. It consumes significantly lower power than other members of the TMS320C6000™ platform of DSPs.

On-Chip Features:

* TMS320C674x Fixed/Floating-Point VLIW DSP Core
* 64 General-Purpose Registers (32 Bit)
* Six ALU (32-/40-Bit) Functional Units
* Two Multiply Functional Units
* Instruction Packing Reduces Code Size
* All Instructions Conditional
* Hardware Support for Modulo Loop Operation
* Real time clock

On-Chip Memory:

* Two Level Cache Memory Architecture
* 32K-Byte L1P Program RAM/Cache
* 32K-Byte L1D Data RAM/Cache
* 256K-Byte L2 Unified Mapped RAM/Cache
* 128K-Byte RAM Shared Memory

On-Board Features:

* 2 Meg x 16 Bit x 4 Banks Synchronous DRAM for External Program/Data
* **Codec:**
  * Stereo Audio ADC & DAC
  * 16/20/24/32-Bit Data Format
  * Supports Rates From 8 kHz to 96 kHz
  * Programmable Input /Output Analog Gains
  * Audio Serial Data Bus Supports I2S, Left/Right-Justified, DSP, and TDM Modes

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* **On Board ADC/DAC**
  * **ADC:**
    - # No of ADC input : 2 Channels
    - # Resolution : 12 bit
    - # Sampling rate : 1Msps (max)
    - # Analog input range : + 5V (max)
    - # High speed SPI serial interface
  - **DAC:**
    - * No of DAC output : 2 Channels
    - * Resolution : 12 bit
    - * Settling time : 8.5 micro sec (max)
    - * Analog output range : + 5V (max)
    - * High speed SPI serial interface
* **Extra Features:**
  - * Provision to connect external JTAG Emulator
  - * 8 user definable LEDs
  - * 8 position DIP switch, user definable
  - * Two 3.5 mm. audio jacks for audio IN and OUT
  - * Expansion connector for GPIO / Video Add on card
* **JTAG Emulator (XDS100V1):**

  Emulation Connect/Disconnect, Read/Write memory, Read registers, Load program, Run, Halt, Step, Software and Hardware Breakpoint support, Real-Time Mode. Support for USB Full Speed (12 Mbits/s)

List of Deliverables:

* **Hardware**
  - o VSK – 6748 Trainer Kit
  - o Microphone, Speaker
  - o USB Cable
  - o Power Supply +5V Adaptor
  - o Software CD
  - o Program & Manual CD

Warranty : 1 Year

No of items : 3 numbers

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