

RICHU NORMAN

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OBJECTIVE

Innovative Research Scholar specializing in compiler optimization, RISC-V architecture, and LLVM development with 4+ years of experience. Seeking roles in compiler engineering, system architecture, and performance optimization to drive innovation in modern computing systems.

EDUCATION

PhD in Computer Science (Pursuing), Cochin University of Science and Technology Oct 2021 - Present
Focus: Compiler Optimization, RISC-V Architecture, ML-based Optimization Frameworks

M.Tech in Computer and Information Science, Cochin University of Science and Technology 2016 - 2018
CGPA: 8.53/10 (81%) — Rank: 2nd in batch

B.Tech in Computer Science and Engineering, Albertian Institute of Science and Technology 2012 - 2016
Mahatma Gandhi University — CGPA: 8.01/10 (77%)

SKILLS

Compiler Development	LLVM Backend Development, RISC-V ISA, Compiler Optimization
Programming Languages	C, C++, Python, Java, SQL, PHP
Technologies	Embedded Systems, IoT, Microsoft Azure, AWS, Android Development, ASP.NET
Tools & Platforms	Visual Studio, Android Studio, SSMS, Linux, Windows, MongoDB
Research Areas	Compiler Optimization, Computer Architecture, Data Science

EXPERIENCE

Research Scholar Oct 2021 - Present
Cochin University of Science and Technology *Kochi, Kerala, India*

- Developing custom compiler passes in LLVM for RISC-V backends, implementing bit manipulation and PSIMD extensions to enhance C code efficiency and benchmarking
- Leading Compiler implementation for optimization framework research for Bitmanipulation, AI/ML workloads targeting RISC-V processors under Chip to Semiconductor Industry(C2S) project funded by Ministry of Electronics and IT
- Contributing to compiler backend development and instruction set extensions, publishing technical papers and proposals at international conferences

ACM India Aneshansetu Fellow Apr 2024 - Apr 2025
Indian Institute of Technology, Kanpur (Under Prof. Dr. Amey Karkare) *Kanpur, UP, India*

- Selected for prestigious ACM fellowship focusing on advanced compiler optimization techniques and RISC-V architecture research
- Collaborating on cutting-edge compiler technologies and performance optimization frameworks

Assistant Professor Aug 2018 - Oct 2021
Various Institutions (St. Paul's College, College of Engineering Cherthala) *Kerala, India*

- Taught core computer science courses including Data Structures, Machine Learning, Embedded Systems, and Computer Architecture
- Mentored 50+ students in research projects, achieving 90% placement rate in top tech companies

Research Intern May 2017 - Apr 2018
ITC Infotech *Bangalore, India*

- Developed IoT-based retail customer experience solution using BLE Beacons, QR codes, and sensor modules, deployed in 5+ retail stores
- Built Outlook plugin for automated email extraction and order placement using computer vision and NLP, reducing manual processing time by 60%
- Implemented solutions using Azure Cloud API, AWS, and ASP.NET Web API

PROJECTS

DSP and AI Workload Tuned Embedded RISC-V Processors. MeitY-funded project (EE-9/2/2021-R&D-E) awarded to CUSAT and Incore Semiconductors. Developed compiler backend for RISC-V instruction set extensions and optimizing compiler, achieving 30%+ performance improvements for AI/ML workloads.

Retail Customer Experience Based on IoT. Built comprehensive IoT solution for retail stores using BLE Beacons, QR codes, and sensor modules. Deployed across multiple retail locations, enhancing customer engagement and analytics.

Email Extraction for Order Placement. Developed Outlook plugin using computer vision and NLP to automatically extract email content and process images for cargo order placement, reducing processing time by 60%.

Smart Review & Sixth Sense. Created web application for automated review generation and desktop application for mouseless interaction using camera and color markers, demonstrating innovation in HCI.

ACHIEVEMENTS & CERTIFICATIONS

- ACM Aneshansetu Fellowship Awardee 2024-25 under Prof. Dr. Amey Karkare, IIT Kanpur
- Secured 2nd Rank in M.Tech Computer and Information Science, CUSAT (2016-18 batch)
- Qualified UGC-NET (Dec 2018, Dec 2022), GATE Computer Science 2022, and GATE Data Science 2023
- Presented research at 12th International Conference on Intelligent Systems and Embedded Design (ISED-2024), NIT Rourkela

PUBLICATIONS & CONFERENCES & WORKSHOPS ATTENDED

- Participated in ACM India Innovations in Compiler Technology (IICT) Workshop, IISc Bangalore, September 2025
- Presented at 12th International Conference on Intelligent Systems and Embedded Design (ISED-2024), NIT Rourkela, Dec 2024
- Participated in ACM India Grant Cohort 2024, IIT Hyderabad, July 2024
- Attended FDP on Microarchitecture Evaluation Tools, NIT Calicut (Aug 2025)