FACULTY PROFILE

<table>
<tr><td>Name: PRAMOD P.</td><td rowspan="2">Address: UPASANA, NEAR EMS MANDIRAM, KOVVAL STORE,
KANHANGAD SOUTH P.O.,
KASARAGOD DISTRICT</td></tr>
<tr><td rowspan="2">Designation:
Assistant Professor</td></tr>
<tr><td>Email: pramodp2006@gmail.com</td></tr>
<tr><td>Department: ECE</td><td>Mobile: 9447855635</td></tr>
<tr><td colspan="2">ACADEMIC QUALIFICATIONS</td></tr>
<tr><td>Doctoral (Institute, year, Subject)</td><td>Pursuing Ph.D(Division of Electronics, School of Engineering, Cochin University of Science and Technology (CUSAT), Kerala, India.)</td></tr>
<tr><td>P.G.</td><td>M.E.VLSI DESIGN, ANNA UNIVERSITY, 2012</td></tr>
<tr><td>U.G.</td><td>B.E. ECE, MADRAS UNIVERSITY, 2000</td></tr>
<tr><td>Other qualifications</td><td>MBA- ICFAI University.

Executive Program for Young Professionals (post graduate management program) - IIM Calcutta</td></tr>
<tr><td colspan="2">AREA OF INTEREST</td></tr>
<tr><td colspan="2">Digital System Design, Low Power Techniques, VLSI Design & Testing, and VLSI Signal Processing.</td></tr>
<tr><td colspan="2">WORK EXPERIENCE</td></tr>
</table>

Teaching (*Period, position, Organization*)	Assistant Professor, ECE Department, LBS College of Engineering, Kasaragod (11/09/2002 to till date)
Industry	---
Others	---
RECENTLY TAUGHT COURSES	
MEMS, ASIC DESIGN, VLSI DESIGN, LOW POWER VLSI, CONTROL SYSTEMS, VLSI SIGNAL PROCESSING, CMOS VLSI, DIGITAL SYSTEM DESIGN	
OTHER RESPONSIBILITIES	
PUBLICATIONS (LATEST)	
Peer Reviewed Science cited International Journals	1. Pramod P, Shahana, T.K., " Exact and approximate multiplications for signal processing applications ", Microelectronics Journal, Elsevier, Volume 132, February 2023, 105688 (Science Citation Index (SCI) Expanded) 2. Pramod P and Shahana, T.K., "High Throughput and Energy Efficient Linear Phase FIR Filter Architectures." *Microprocessors and Microsystems*, Elsevier, *vol. 87, Nov. 2021*, 104367. https://doi.org/10.1016/j.micpro.2021.104367 (Science Citation Index (SCI)) 3. Pramod P and Shahana, T.K., "An efficient architecture for signed carry save multiplication", IEEE letters of computer society, Vol. 3, No. 1, pp. 9-12, January–June 2020, https://doi.org/10.1109/LOCS.2020.2971443 4. Pramod P, Shahana T.K., "Efficient modular hybrid adders and Radix-4 booth multipliers for DSP applications", Microelectronics Journal, Elsevier, vol.96, feb. 2020, 104701, https://doi.org/10.1016/j.mejo.2020.104701 (Science Citation Index (SCI) Expanded) 5. Pramod P, Shahana T.K., "High throughput FIR filter architectures using retiming and modified CSLA based adders", IET

	Circuits,Devices and Systems, vol. 13, no. 7, pp. 1007-17, 2019, https://doi.org/10.1049/iet-cds.2019.0130 (Science Citation Index (SCI)) 6. Pramod P., Shahana T. K., "Delay and Energy Efficient Modular Hybrid Adder for Signal Processor Architectures", IETE Journal of Research - Taylor & Francis, 2 June 2019, https://doi.org/10.1080/03772063.2019.1627917 *(Science Citation Index (SCI) Expanded)* 7. Pramod P, Shahana, T.K., "High throughput adaptive filter architecture using modified transpose form FIR filters", Journal of Advanced Research in Dynamical and Control Systems, vol. 10, no. 15, pp. 68-82, Nov. 2018, ISSN 1943023X, *(Scopus indexed)* 8. Pramod P. and Shahana T.K., "High throughput and energy efficient FIR filter architectures using retiming and two level pipelining", Procedia Computer Science (Elsevier), Volume 171, 2020, Pages 617-626
Peer Reviewed Science cited International Conferences	1)Pramod P. and Shahana T.K., "High throughput and energy efficient FIR filter architectures using retiming and two level pipelining", Third International Conference on Computing and Networking Communications (COCONET), Thiruvananthapuram, 18-20, December 2019

Date: 21 06 23 Signature: